REMARKS

If a petition for an extension of time is required to make this preliminary amendment timely, this paper should be considered to be such a petition, and the Commissioner is authorized to charge the requisite fees to our Deposit Account No. 03-3125. The Office is hereby authorized to charge any additional fees that may be required in connection with this amendment and to credit any overpayment to our Deposit Account No. 03-3125.

If a further telephone interview could advance the prosecution of this application, the Examiner is respectfully requested to call the undersigned attorney.

Entry of this preliminary amendment and allowance of this application are respectfully requested.

Respectfully submitted,

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EXHIBIT A

1. (Amended) A flash memory device comprising:

a first flash memory array having a first predetermined number of blocks; and

a second flash memory array having a second predetermined number of blocks and sharing input/output lines with the first flash memory array, wherein the first predetermined number of blocks is different than the second predetermined number of blocks, wherein more than two of the blocks of the first flash memory array are minimum erasing units of the flash memory device, and wherein a read operation is enabled in the second [first] flash memory array when the first [second] flash memory array is written or erased.

5. (Amended) A flash memory device comprising:

a first flash memory array having a first number of blocks of storage capacity; and

a second flash memory array having a second number of blocks of storage capacity and sharing input/output lines with the first flash memory array, wherein the first number of blocks is different than the second number of blocks, wherein more than two of the blocks of the first flash memory array are minimum erasing units of the flash memory device, and wherein the second [first] flash memory array is capable of being read when the first [second] flash memory array is written or erased.

8. (Amended) A flash memory including an array of blocks divided into multiple areas, said flash memory comprising:

a first flash memory area having a first number of blocks; and

a second flash memory area having a second number of blocks and sharing input/output lines with the first flash memory area, wherein the first number of blocks is different than the second number of blocks, wherein more than two of the blocks of the first flash memory array are minimum erasing units of the flash memory device, and wherein while programming or erasing in the first [second] flash memory area, read operations are possible in the second [first] flash memory area.

12. (Amended) The flash memory device as recited in claim 11, wherein while programming or erasing in the first [second] flash memory area, read operations are possible in the second [first] flash memory area.

13. (Amended) A flash memory device comprising:

a first flash memory array having a first predetermined number of sectors; and

a second flash memory array having a second predetermined number of sectors and

sharing input/output lines with the first flash memory array, wherein the first predetermined number of sectors is different than the second predetermined number of sectors, wherein more than two of the sectors of the first flash memory array are minimum erasing units of the flash memory device, and wherein a read operation is enabled in the second [first] flash memory array when the first [second] flash memory array is written or erased.

17. (Amended) A flash memory device comprising:

a first flash memory array having a first number of sectors of storage capacity; and

a second flash memory array having a second number of sectors of storage capacity and sharing input/output lines with the first flash memory array, wherein the first number of sectors is different than the second number of sectors, wherein more than two of the sectors of the first flash memory array are minimum erasing units of the flash memory device, and wherein the second [first] flash memory array is capable of being read when the first [second] flash memory array is written or erased.

20. (Amended) A flash memory including an array of storage divided into multiple areas, said flash memory comprising:

a first flash memory area having a first number of sectors; and

a second flash memory area having a second number of sectors and sharing input/output lines with the first flash memory area, wherein the first number of sectors is different than the second number of sectors, wherein more than two of the sectors of the first flash memory array are minimum erasing units of the flash memory device, and wherein while programming or erasing in the first [second] flash memory area, read operations are possible in the second [first] flash memory area.

EXHIBIT B

1. (Amended) A flash memory device comprising:

a first flash memory array having a first predetermined number of blocks; and

a second flash memory array having a second predetermined number of blocks and sharing input/output lines with the first flash memory array, wherein the first predetermined number of blocks is different than the second predetermined number of blocks, wherein more than two of the blocks of the first flash memory array are minimum erasing units of the flash memory device, and wherein a read operation is enabled in the second flash memory array when the first flash memory array is written or erased.

5. (Amended) A flash memory device comprising:

a first flash memory array having a first number of blocks of storage capacity; and

a second flash memory array having a second number of blocks of storage capacity and sharing input/output lines with the first flash memory array, wherein the first number of blocks is different than the second number of blocks, wherein more than two of the blocks of the first flash memory array are minimum erasing units of the flash memory device, and wherein the second flash memory array is capable of being read when the first flash memory array is written or erased.

8. (Amended) A flash memory including an array of blocks divided into multiple areas, said flash memory comprising:

a first flash memory area having a first number of blocks; and

a second flash memory area having a second number of blocks and sharing input/output lines with the first flash memory area, wherein the first number of blocks is different than the second number of blocks, wherein more than two of the blocks of the first flash memory array are minimum erasing units of the flash memory device, and wherein while programming or erasing in the first flash memory area, read operations are possible in the second flash memory area.

12. (Amended) The flash memory device as recited in claim 11, wherein while programming or erasing in the first flash memory area, read operations are possible in the second flash memory area.

13. (Amended) A flash memory device comprising:

a first flash memory array having a first predetermined number of sectors; and

a second flash memory array having a second predetermined number of sectors and sharing input/output lines with the first flash memory array, wherein the first predetermined

number of sectors is different than the second predetermined number of sectors, wherein more than two of the sectors of the first flash memory array are minimum erasing units of the flash memory device, and wherein a read operation is enabled in the second flash memory array when the first flash memory array is written or erased.

17. (Amended) A flash memory device comprising:

a first flash memory array having a first number of sectors of storage capacity; and

a second flash memory array having a second number of sectors of storage capacity and sharing input/output lines with the first flash memory array, wherein the first number of sectors is different than the second number of sectors, wherein more than two of the sectors of the first flash memory array are minimum erasing units of the flash memory device, and wherein the second flash memory array is capable of being read when the first flash memory array is written or erased.

20. (Amended) A flash memory including an array of storage divided into multiple areas, said flash memory comprising:

a first flash memory area having a first number of sectors; and

a second flash memory area having a second number of sectors and sharing input/output lines with the first flash memory area, wherein the first number of sectors is different than the second number of sectors, wherein more than two of the sectors of the first flash memory array are minimum erasing units of the flash memory device, and wherein while programming or erasing in the first flash memory area, read operations are possible in the second flash memory area.